



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/930,030	08/14/2001	Claude R. Gauthier	03226/106001;P6086	1932
32615	7590	04/29/2004	EXAMINER	
OSHA & MAY L.L.P./SUN 1221 MCKINNEY, SUITE 2800 HOUSTON, TX 77010			TRAN, ANH Q	
			ART UNIT	PAPER NUMBER
			2819	

DATE MAILED: 04/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 09/930,030	<b>Applicant(s)</b> GAUTHIER ET AL.	
	<b>Examiner</b> Anh Q. Tran	<b>Art Unit</b> 2819	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 09 February 2004.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1,3-5 and 11 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,3-5 and 11 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                                    |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3-5, and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Teggatz et al (5,424,669).

Claim 1, Teggatz shows apparatus for reducing a magnitude of a rate of current change of an integrated circuit, comprising:

A control stage (21, 23, Fig. 2) that generates a control signal indicative of whether power consumption by the integrated circuit needs to be reduced; and

a counter stage (43, 35-41) that inputs the control signal and generates to a plurality signals to a plurality of transistors (27-33), wherein the plurality of signals sequentially disable the plurality of transistors to cause a gradual reduction in an amount of current sourced from a power terminal to a ground terminal of the integrated circuit (**the same procedure can be used when turning off power output device 24,** col. 3, lines 40-60, therefore the plurality of signals sequentially disable the plurality of transistors to cause a gradual reduction in an amount of current source since the same procedure is applied when turning off power).

Claim 3, Tegatz shows the counter stage enables the plurality of transistors when power consumption by the integrated circuit does not need to be reduced (col. 4, lines 1-18).

Claim 4, Tegatz shows the plurality of transistors are a n-type transistor.

Claim 5, Tegatz shows a circuit for reducing a rate of current change of a microprocessor (Fig. 2), comprising:

A control stage (21, 23, Fig. 2) that is connected to a power terminal and a ground terminal, wherein the control stage generates a control signal that is indicative of whether power consumption by the microprocessor needs to be reduce; and

A counter stage (43, 35-41) that inputs the control signal and a clock signal (oscillator time period, col. 3, line29), wherein the counter stage is arranged to generate a plurality of signals to a plurality of transistors (27-33) connected in parallel across the power terminal (VDD) and the ground terminal (GND),

Wherein, dependent on the control signal, the plurality of signals are generated to sequentially disable the plurality of transistors to cause a gradual reduction in an amount of current sourced from the power terminal to the ground terminal by the plurality of transistors (**the same procedure can be used when turning off power output device 24**, col. 3, lines 40-60, therefore the plurality of signals sequentially disable the plurality of transistors to cause a gradual reduction in an amount of current source since the same procedure is applied when turning off power).

Art Unit: 2819

Claim 11, Tegatz shows the plurality of transistors, when in an enabled state, source substantially a maximum amount of current from the power terminal to the ground terminal (col. 4, lines 1-18).

***Conclusion***

3. Applicant's arguments filed 2/9/04 have been fully considered but they are not persuasive. Tegatz shows all the features of the present invention because in col. 3, line 59-60, Tegatz teaches that "the same procedure can be used when turning off power output device 24", therefore, the plurality of signals sequentially disable the plurality of transistors to cause a gradual reduction in an amount of current source is applied when turning off power.

4. Furthermore, Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

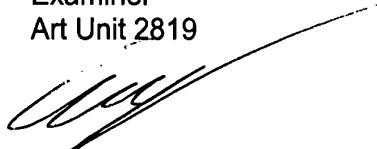
the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-TH (7:00-5:30) Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Anh Q. Tran  
Examiner  
Art Unit 2819



4/21/04